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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/003,170	11/14/2001	Eugene P. Matter	42390P12396	7336

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EXAMINER	
MCLEAN MAYO, KIMBERLY N	
ART UNIT	**PAPER NUMBER**
2187	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/003,170	MATTER ET AL.	
	Examiner	Art Unit	
	Kimberly N. McLean-Mayo	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *April 14, 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4,6-10,12 and 16-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,3,4 and 6-9* is/are allowed.

6)☒ Claim(s) *10,12 and 16-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In view of the Appeal Brief filed on April 14, 2006, PROSECUTION IS HEREBY REOPENED. A detailed action is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 10, 12, 16 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Uchiyama et al. (USPN: 5,140,681).

Regarding claims 10 and 12, Uchiyama discloses individual memory device including a memory array (Figure 5; Figure 2, Reference 5) having a first portion (Figure 5, Reference 61) and a second portion (Figure 5, Reference 62); a first processor (Figure 5, Processor 1; C 5, L 28-31) and a second processor (Figure 5, Processor 2; C 5, L 30-31), wherein the first portion of the memory array is directly accessible only by the first processor via a first bus, (the first processor accesses the first portion of the memory via the bus coupled to Reference 3 and Reference 7 in Figure 2, wherein Reference 7 is also coupled to Reference 5 in Figure 2); and the second portion of the memory array is directly accessible only by the second processor via a second bus (the second processor accesses the second portion of the memory via the bus coupled to Reference 4 and Reference 7 in Figure 2, wherein Reference 7 is also coupled to Reference 5 in Figure 2).

Regarding claim 16, Uchiyama discloses wherein the memory array further comprises a third portion that is different than the first portion and the second portion (Figure 5, References 60 and 63), the third portion of the memory array accessible by both the first processor and the second processor (C 5, L 26-28).

Regarding claim 21, Uchiyama discloses the memory comprises memory selected from the group consisting of static random access memory, dynamic random access memory, read only memory, electrically erasable and programmable read only memory and flash memory (Uchiyama discloses a memory device which encompasses any memory device).

4. Claims 10, 12 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Miller et al. (USPN: 6,212,607).

Regarding claims 10, 12 and 21, Miller discloses an individual memory device including a memory array having a first portion (selected memory banks of the array in which the first processor has been granted exclusive access to; Figure 3, Reference 301) and a second portion (selected memory banks of the array in which the second processor has been granted exclusive access to plurality of memory banks; Figure 3, Reference 301); a first processor (Figure 2, Reference 205); and a second processor (Figure 2, Reference 206), wherein the first portion of the memory array is directly accessible only by the first processor via a first bus (Figure 2, Reference 203; C 21, L 26-30, L 49-59); and the second portion of the memory array is directly accessible only by the second processor via a second bus (Figure 2, Reference 204; C 21, L 26-30, L 49-59; same process is performed for Reference 206 in Figure 2).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Uchiyama et al. (USPN: 5,140,681) in view of Yokota (USPN: 4,930,066).

Uchiyamam discloses the limitations cited above, additionally Uchiyama discloses the first and second portions of the memory coupled to a same power supply potential (the memory portions

are part of a single memory device and thus are coupled to the same potential as the memory device), however, Uchiyama does not explicitly disclose the memory portions coupled to a same clock signal. Yokota discloses memory portions coupled to a same clock (Figure 2). This feature taught by Yokota provides synchronization and provides memory access at the speed of the clock thereby improving the performance of the system. Hence, it would have been obvious to one of ordinary skill in the art to couple the memory portions in the system taught by Uchiyama to a same clock for the desirable purpose of improved performance.

7. Claims 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uchiyama et al. (USPN: 5,140,681) in view of Blumrich (USPN: 6,493,800).

Regarding claims 18-19, Uchiyama does not disclose dynamically altering a size of the first and second portion of the memory array depending on an operational load of the first and second processor. However, Blumrich discloses dynamically altering a size of the first portion and the second portion of a memory array depending on an operational load of the first and second processor (C 2, L 29-43; C 6, L 61-67; C 7, L 1-67). This feature taught by Blumrich provides improved performance by providing efficient memory usage based on the operating conditions of the system. Hence, it would have been obvious to one of ordinary skill in the art to use Blumrich's teachings with the system taught by Uchiyama for the desirable purpose of improved performance and efficiency.

8. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Uchiyama et al. (USPN: 5,140,681) in view of Cherabuddi (PGPUB: US 2202/0184445).

Uchiyma discloses the limitations cited above, however, Uchiyama does not disclose the first processor accessing the first portion of the memory array substantially simultaneously as the second processor access the second portion of the memory array. However, Cherabuddi discloses the first processor accessing the first portion of the memory array substantially simultaneously as the second processor access the second portion of the memory array (pages 3-4, section [0034]; - the first and second processor are granted exclusive access simultaneously to the first and second amount of memory and thus the first processor may read to the first portion of memory simultaneous with the second processor writing to the second portion of memory). This feature taught by Cherabuddi improves the performance of the system by processing multiple instruction/processes at the same time. One of ordinary skill in the art would have recognized this benefit afforded by Cherabuddi's teachings and would have been motivated to use Cherabuddi's teachings in the system taught by Uchiyama for the desirable of purpose of improved performance.

Response to Arguments

9. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

However, regarding Applicant's argument that Uchiyama discloses accessing the first and second portions of memory via a main system bus, Uchiyama discloses the first and second processors accessing the first and second portion of memory respectively via first and second buses which are coupled to the main bus. The language/scope of the claim does not indicate that

the first and second processors access the first and second portions of memory directly via the first and second bus, without any intervening logic or communication paths.

Allowable Subject Matter

10. Claims 1, 3-4 and 6-9 are allowed.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly N. McLean-Mayo whose telephone number is 571-272-4194. The examiner can normally be reached on Monday – Friday between the hours of 10-6:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 571-272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Kimberly N. McLean-Mayo

KIMBERLY MCLEAN-MAYO
PRIMARY EXAMINER

DONALD SPARKS
SUPERVISORY PATENT EXAMINER